IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	:	Attorney Docket No. 2004_1091A
Syuji MATSUDA et al.	:	**Confirmation No. 5201**
Serial No. 10/501,150	:	Group Art Unit 2112
Filed July 13, 2004	:	Examiner Joseph D. Torres
INTERLEAVED DATA ERROR CORRECTION METHOD DEVICE	:	**Mail Stop: APPEAL BRIEFS-PATENTS**

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following is Appellant's Brief, submitted under the provisions of 37 CFR 41.37.

Pursuant to the provisions of 37 CFR 41.20, this Brief is submitted with a fee of $540.00.

The USPTO is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16, 1.17, and 1.492, which may be required by this paper to Deposit Account No. 23-0975.

REAL PARTY IN INTEREST

The real party in interest is Panasonic Corporation (formerly known as Matsushita Electric Industrial Co., Ltd). of Osaka, Japan.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 17-26, 37 and 38 stand finally rejected.

The Appellant appeals the final rejection of claims 17-26, 37 and 38.

STATUS OF AMENDMENTS

No amendments were filed subsequent to the Final Office Action of April 19, 2010.

SUMMARY OF CLAIMED SUBJECT MATTER

A concise explanation of the subject matter defined in each of the independent claims is presented below with reference to the written description (see the substitute specification filed on November 5, 2007) of this application.

The subject matter of independent claim 17 is directed to an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information, the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising: judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved; configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte

of main data were both located between the first and second bytes of sub data before being deinterleaved, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data; and performing error correction on the error correction target code line (see Figs. 4(b), 5, 7 and 8; page 13, lines 5-20; page 14, line 12 through page 15, line 4; page 15, line 12 through page 18, line 11; and page 24, lines 1-20).

The subject matter of independent claim 18 is directed to an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information, the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising: judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved; configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data; and performing error correction on the error correction target code line, wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second

sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area, wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved (see Figs. 4(b), 5, 7 and 8; page 13, lines 5-20; page 14, line 12 through page 15, line 4; page 15, line 12 through page 18, line 11; and page 24, lines 1-20).

The subject matter of independent claim 19 is directed to an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information, the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising: judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved; configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data; and performing error correction on the error correction target code line, wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals (see Figs. 4(b), 5, 7 and 8; page 13, lines 5-20; page 14, line 12 through page 15, line 4; page 15, line 12 through page 18, line 11; and page 24, lines 1-20).

The subject matter of independent claim 22 is directed to an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to

configure erasure position information, the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising: judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information; configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon coded data; and performing error correction on the error correction target code line (see Figs. 4(b), 5, 7 and 8; page 13, lines 5-20; page 14, line 12 through page 15, line 4; page 15, line 12 through page 18, line 11; and page 24, lines 1-20).

The subject matter of independent claim 23 is directed to an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information, the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising: judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information; configuring erasure position information of said first byte of main data belonging to the error correction

target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon coded data; and performing error correction on the error correction target code line, wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area, wherein the second sub data area is disposed between the first main data area and the second main data area, and wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved (see Figs. 4(b), 5, 7 and 8; page 13, lines 5-20; page 14, line 12 through page 15, line 4; page 15, line 12 through page 18, line 11; and page 24, lines 1-20).

The subject matte recited in independent claim 24 is directed to an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information, the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising: judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of

main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information; configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data; and performing error correction on the error correction target code line, wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals(see Figs. 4(b), 5, 7 and 8; page 13, lines 5-20; page 14, line 12 through page 15, line 4; page 15, line 12 through page 18, line 11; and page 24, lines 1-20).

The subject matter of independent claim 37 is directed to an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information, the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising: judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved; configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, the erasure position information being obtained from a position polynomial that is

calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data; and performing error correction on the error correction target code line, wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area, wherein the second sub data area is disposed between the first main data area and the second main data area, wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved, and wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals (see Figs. 4(b), 5, 7 and 8; page 13, lines 5-20; page 14, line 12 through page 15, line 4; page 15, line 12 through page 18, line 11; and page 24, lines 1-20).

The subject matter recited in independent claim 38 is directed to an error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information, the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising: judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information; configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data

belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding of the Reed-Solomon-coded data; and performing error correction on the error correction target code line, wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data, wherein the plurality of main data areas include a first main data area and a second main data area, wherein the plurality of sub data areas include: a first sub data area in which the first byte of sub data is located; a second sub data area in which the second byte of sub data is located; and a third sub data area in which a third byte of sub data is located, wherein the first main data area is disposed between the first sub data area and the second sub data area, wherein the second main data area is disposed between the second sub data area and the third sub data area, wherein the second sub data area is disposed between the first main data area and the second main data area, wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved, and wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals (see Figs. 4(b), 5, 7 and 8; page 13, lines 5-20; page 14, line 12 through page 15, line 4; page 15, line 12 through page 18, line 11; and page 24, lines 1-20).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 17, 19, 20, 22, 24 and 25 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Marchant (US 6,631,492) in view of Nakamura et al. (US 5,684,810) and Kobayashi et al. (US 6,029,264).

B. Claims 18, 23, 37 and 38 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Marchant (US 6,631,492) in view of Nakamura et al. (US 5,684,810) and Kobayashi et al. (US 6,029,264), and further in view of Shutoku et al. (US 7,089,401).

C. Claims 21 and 26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Marchant (US 6,631,492) in view of Nakamura et al. (US 5,684,810) and Kobayashi et al. (US 6,029,264), and further in view of Eachus (US 3,685,016).

ARGUMENT

I. Rejection of claims 17, 19, 20, 22, 24 and 25 under 35 U.S.C. § 103(a) over Marchant (US 6,631,492) (hereinafter "Marchant") in view of Nakamura et al. (US 5,684,810) (hereinafter "Nakamura") and Kobayashi et al. (US 6,029,264) (hereinafter "Kobayashi").

Claim 17 recites that the erasure position information is obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data.

Appellants submit that the above-noted feature recited in claim 17 would not have been obvious in view of the teachings of Marchant, Nakamura and Kobayashi.

Regarding the above-noted feature recited in claim 17, Appellants note that in the Final Office Action dated April 19, 2010, the Examiner has recognized that Marchant and Kobayashi do not teach or suggest such a feature. The Examiner, however, has applied Nakamura, and has taken the position that it would have been obvious to modify Marchant, based on the disclosure in Nakamura, so as to provide such a feature.

In particular, in the Response to Arguments section of the Final Office Action dated April 19, 2010 (see the Final Office Action at page 3, line 20 through page 4, line 1), the Examiner has set forth the following:

> "Nakamura teaches that in Reed-Solomon Erasure decoding erasures are erasure flagged during <u>C1 inner/row code decoding</u> <u>**just as in Marchant**</u>. However, Nakamura provides details missing in Marchant as to how erasure flagging is executed." (emphasis added).

In response to the above-noted comments made by the Examiner, Appellants submit that the Examiner's understanding of Marchant is incorrect. In particular, Appellants note that Figs.

5-7 in Marchant do **not** relate to a product code, and therefore, Appellants submit that there is clearly no concept of "decoding of C1 inner/row code" in these figures of Marchant.

In this regard, Appellants note that while Figs. 5-7 of Marchant perform detection of erasure by scratch detection fields (e.g., see col. 6, lines 28-56 of Marchant), that Figs. 5-7 of Marchant do not perform detection of erasure by inner code.

Thus, because Marchant merely performs detection of erasure by scratch detection fields, Appellants submit that it would be impossible to combine Figs. 5-7 of Marchant, which do not relate to the product code, with Nakamura, which relates to a decoding method for decoding the product code comprising the inner code and the outer code.

In other words, Appellants submit that because Marchant performs detection of erasure by scratch detection fields, and does not perform detection of erasure by inner code, that combining Marchant and Nakamura in the manner suggested by the Examiner would render Marchant either inoperable, or unsatisfactory, for its intended principle of operation, which is performing detection of erasure by scratch detection fields. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125. In addition, Appellants submit that there would have been no motivation or suggestion to combine Marchant and Nakamura, as the Examiner suggests, because doing so would change the principle of operation of Marchant because such a combination would prevent Marchant from performing detection of erasure by scratch detection fields. *In re Ratti*, 123 USPQ 349 (CCPA 1959).

In view of the foregoing, Appellants submit that the Examiner's position regarding the obviousness of combining Marchant and Nakamura is incorrect.

Accordingly, Appellants submit that the combination of Marchant, Nakamura, and Kobayashi does not render obvious at least the above-noted feature recited in claim 17 which indicates that that the erasure position information is obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data.

Therefore, Appellants submit that claim 17 is patentable over the combination of Marchant, Nakamura, and Kobayashi, an indication of which is requested.

Regarding claims 19, 22 and 24, Appellants note that each of these claims recites that the erasure position information is obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data.

For at least the same reasons as discussed above with respect to claim 17, Appellants submit that the combination of Marchant, Nakamura, and Kobayashi does not render obvious the above-noted feature recited in claims 19, 22 and 24. Accordingly, Appellants submit that claims 19, 22 and 24 are patentable over the cited prior art, an indication of which is requested.

Regarding claims 20 and 25, Appellants note that claim 20 depends from claim 19 and that claim 25 depends from claim 24. Accordingly, Appellants submit that claims 20 and 25 are patentable at least by virtue of their dependency.

II. Rejection of claims 18, 23, 37 and 38 under 35 U.S.C. § 103(a) over Marchant (US 6,631,492) (hereinafter "Marchant") in view of Nakamura et al. (US 5,684,810) (hereinafter "Nakamura") and Kobayashi et al. (US 6,029,264) (hereinafter "Kobayashi"), and further in view of Shutoku et al. (US 7,089,401) (hereinafter "Shutoku").

Regarding claims 18, 23, 37 and 38, Appellants note that each of these claims recites that the erasure position information is obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data.

For at least the same reasons as discussed above with respect to claim 17, Appellants submit that the combination of Marchant, Nakamura, and Kobayashi does not render obvious the above-noted feature recited in claims 18, 23, 37 and 38. Further, Appellants submit that Shutoku does not cure the above-noted deficiencies of Marchant, Nakamura, and Kobayashi.

Accordingly, Appellants submit that claims 18, 23, 37 and 38 are patentable over the cited prior art, an indication of which is requested.

III. Rejection of claims 21 and 26 under 35 U.S.C. § 103(a) over Marchant (US 6,631,492) (hereinafter "Marchant") in view of Nakamura et al. (US 5,684,810) (hereinafter "Nakamura") and Kobayashi et al. (US 6,029,264) (hereinafter "Kobayashi"), and further in view of Eachus (US 3,685,016) (hereinafter "Eachus").

Claim 21 depends from claim 19, and claim 26 depends from claim 24. Appellants submit that Eachus does not cure the above-noted deficiencies of Marchant, Nakamura, and Kobayashi, with respect to claims 19 and 24. Accordingly, Appellants submit that claims 21 and 26 are patentable at least by virtue of their dependency.

Conclusion

For the reasons set forth above, Appellants respectfully submit that the combination of Marchant, Nakamura, Kobayashi, and Shutoku and Eachus does not render obvious all of the features recited in claims 17-26, 37 and 38. Accordingly, Appellants submit that claims 17-26, 37 and 38 are patentable over the prior art of record.

Respectfully submitted,

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By 2010.12.29 14:51:57 -05'00'

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CLAIMS APPENDIX - Claims on Appeal

17. An error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data; and

performing error correction on the error correction target code line.

18. An error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data

which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data; and

performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area, and

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved.

19. An error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data; and

performing error correction on the error correction target code line,

wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

20. An error correction method as defined in Claim 19, wherein said judging judges that the first byte of main data and the second byte of main data do not exist between the first and second bytes of sub data when said first byte of main data is directly subsequent to a byte of sub data or a byte of sync data in a data recording order.

21. An error correction method as defined in Claim 20, wherein said performing error correction performs error correction without using said erasure position information when an amount of said erasure position information configured in said configuring of erasure position information is higher than an amount of parity data.

22. An error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data

which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising:

judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon coded data; and

performing error correction on the error correction target code line.

23. An error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data

which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising:

judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon coded data; and

performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data

of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area, and

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved.

24. An error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising:

judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data; and

performing error correction on the error correction target code line,

wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

25. An error correction method as defined in Claim 24, wherein said judging judges that the first byte of data and the second byte of main data do not exist between the first and second bytes of sub data when said first byte of main data is directly subsequent to a byte of sub data or a byte of sync data in a data recording order.

26. An error correction method as defined in Claim 25, wherein said performing error correction performs error correction without using said erasure position information when an amount of said erasure position information configured in said configuring of erasure position information is higher than an amount of parity data.

37. An error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding on the Reed-Solomon-coded data; and

performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area,

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved, and

wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

38. An error correction method for an error correction code (ECC) block that includes Reed-Solomon-coded data, said error correction method using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said error correction method comprising:

judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information, the erasure position information being obtained from a position polynomial that is calculated at a time of performing Reed-Solomon decoding of the Reed-Solomon-coded data; and

performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area,

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved, and

wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.